

ETS 2019

24rd IEEE European Test Symposium

May 27 - May 31, 2019
Baden-Baden, Germany

Program





GEMEINSAM IN DIE ZUKUNFT – GESTALTEN WIR DIE WELT VON MORGEN

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Program Guide

PROGRAM

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Welcome

On behalf of the Program, Organizing, and Steering Committees, we would like to extend a warm welcome to everyone attending the European Test Symposium 2019. ETS has been established as one of the main international forums and the largest one in Europe that brings together the test community to present and discuss scientific results, emerging ideas, applications, hot topics, and new trends in the area of electronic-based circuit and system testing and reliability as well as in the fields of verification and security aspects in test. Topics of interest include but are not limited to, design-for-test, dependability, security, failure analysis and diagnosis, on-line test, automated test hardware, validation and verification, fault simulation, fault tolerance, automatic test generation, test of emerging architectures and technologies, etc.

This year ETS takes place in Baden-Baden, Germany, and is organized by the Karlsruhe Institute of Technology (KIT), which co-

sponsors the event jointly with the IEEE Council on Electronic Design Automation (CEDA). Baden-Baden was established over 2,000 years ago as a place for people to relax and reconnect with themselves. Water, light, earth, and air are the city's precious resources. As the pearl of the Black Forest, extraordinary hot springs, spas and nature, hotels of unparalleled quality – and the lure of the casino, are among its attractions. Over the centuries, Baden-Baden has evolved into an enchanting destination, offering a spectacularly diverse range of opportunities for both relaxation and excitement. Its Museum Mile exhibits up-and-coming artists alongside the works of both old and contemporary masters.

ETS is the cornerstone event of the European Test Week, which includes in addition the Test Spring School (TSS) and Fringe Workshops. The main topic for this year's TSS, which precedes the symposium, is Cutting Edge Approaches for Test. Three Fringe Workshops will take place immedi-

ately following ETS'19, namely the 4th International Test Standards Application (TESTA) Workshop, which focuses on test standards, the 8th Workshop on Trustworthy Manufacturing and Utilization of Secure Devices (TRUDEVICE), as well as the Secure Hardware, Integrity and preVention of Attacks Workshop (SHIVA).

ETS'19 received a significant number of scientific paper submissions from 28 countries all over the world. Each paper was evaluated by on average 5 expert reviews. Based on the written reviews and follow-up online discussions among the reviewers, the Organizing Committee and the Topic Chairs convened in Karlsruhe, Germany, on February 8, 2019, and recommended to accept 25 papers for oral presentation, distributed over 9 regular sessions, and 13 papers for poster presentation, distributed over 3 poster sessions. An Award Committee has been formed and will select the best paper based on the reviewers' comments and the ratings provided by the attendees. The authors of the

best paper will receive the Best Paper Award during the opening ceremony of ETS'20.

Apart from scientific paper presentations and posters, the ETS'19 program consists of 3 plenary keynote addresses, 2 one-hour embedded tutorials and 2 TSS@ETS Monday tutorials, 2 panel sessions, 3 special sessions, the PhD contest, and several vendor sessions. In addition, ETS features again a special session on Emerging Test Strategies (ETS²), where new issues are presented by the industry and are discussed in an informal atmosphere. Furthermore, the new Embedded Workshop track is dedicated to work in progress and case studies, while the newly established PhD Forum provides an excellent opportunity for PhD students to present their ongoing work and get feedback from experts in the field.

Finally, the ETS'19 program is enriched with an exciting social program providing superb opportunities for informal discussions among participants in a relaxed setting. The social activities start with a welcome reception and

continue with the main social event on Wednesday. This includes a guided city tour with historical, cultural and music flavors. The social event ends with a relaxing gala dinner at the “Geroldsauer Mühle” in the outskirt of Baden-Baden and the gate to the Black Forest.

ETS’19 is the result of the hard work of many dedicated volunteers involved in the technical and organizational activities leading to the European Test Week. We wholeheartedly thank all of them for their significant effort to put together this edition of ETS. We also thank all authors who submitted their work to ETS’19, the presenters for their contributions, and all attendees for their active participation. We also thank the IEEE Council on Electronic Design Automation and the IEEE Computer Society Test Technology Technical Council for the continued technical sponsorship and support. We particularly thank German Research Foundation - Deutsche Forschungsgemeinschaft (DFG) - for their financial and technical support as well as Karlsruhe Institute of Technology (KIT) for their organizational support. Last but

not least, we extend our thanks to the ETS’19 corporate sponsors: Advantest, ARM, Cadence, Infineon, Intel, Mentor Graphics, Ridgetop Europe and Synopsys, for their financial sponsorship and continued support of ETS.

We are excited about the strong lineup of ETS’19 and overall of the European Test Week. We are confident that you will find it a beneficial and exciting experience with lots of networking opportunities for researchers, developers and vendors. We wish you all a fun-filled and productive week in Baden-Baden!

.....

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Artur Jutman
Jaan Raik
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Program Chair

Görschwin Fey
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Test & Repair for SoC Memories and Hierarchical Test for AMS & PHY IP

Tutorial | Yervant Zorian, Synopsys Fellow |
Wednesday, May 29; 09:15 – 09:45 - Session 7B

Maintaining Automotive Quality for Next-Generation Microcontrollers

Joint Presentation | Vladimir Litovtchenko, Synopsys;
Ralf Arnold, Infineon Technologies; Johanna Sepulveda TU - Munich | Tuesday, May 28;
14:00 – 15:30 - Session 3A

www.synopsys.com/designware-ip

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Dennis Weller (DE)

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arm

Automotive Solutions

Join our talk to discover Arm's latest IP solutions for functional safety applications, including the recently launched Arm Cortex-A76AE.

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General Information

Organizer

Karlsruhe Institute of Technology



Dates / Symposium Venue

Date	May 27 – 31, 2019
Venue	Kongresshaus Baden-Baden Augustaplatz 10 76530 Baden-Baden Germany
Phone	+49 7221 304 -0
Fax	+49 7221 304 -304
Email	info@kongresshaus.de
Web	https://www.kongresshaus.de

Registration / Information Hours

ETS/Workshops

Registration desk (Foyer 1st Floor)

Monday, May 27	13:00 - 19:00
Tuesday, May 28	08:00 - 20:00
Wednesday, May 29	08:00 - 16:00
Thursday, May 30	08:00 - 19:00
Friday, May 31	08:00 - 16:00

Wifi Credentials (Kongresshaus)

SSID : ETS2019
Password: badenETS2019

Proceedings

Web: <https://www.testgroup.polito.it/ets19/proceedings/>
Username: ets2019attendee
Password: 3tspr0c33d1ngs2019

Baden-Baden – The good-good life.

“The Belle Époque Meets The Age Of Instagram” is the headline the New York Times recently used to describe Baden-Baden – and it’s certainly true that today the city’s rich history blends seamlessly with a highly contemporary lifestyle. Baden-Baden was established over 2,000 years ago as a place for people to relax and reconnect with themselves. Water, light, earth and air are the city’s precious resources. Extraordinary hot springs, spas and nature, hotels of unparalleled quality – and the lure of the casino. Over the centuries, Baden-Baden has evolved into an enchanting destination, offering a spectacularly diverse range of opportunities for both relaxation and excitement.

The Pulse Of The Contemporary Can Be Felt Everywhere In Baden-Baden: its Museum Mile exhibits up-and-coming artists alongside the works of both old and contemporary masters; the SWR3 New Pop Festival brings international stars to the city; the Festspielhaus hosts the world’s leading orchestras; new and renowned hotels, restaurants and shops set new standards of excellence for the region – and far beyond. Visitors travel here from all around the world to spend lively nights in the bars and clubs.



Festspielhaus

1

Cognitive Computing: Design, Verification & Security Challenges



Kaushik Roy

*Edward G. Tiedemann Jr.
Distinguished Professor,
Director of the center
for brain-inspired
computing (C-BRIC)*

ABSTRACT:

Deep Learning has made tremendous progress in the recent past; even surpassing humans in some image recognition and gaming tasks. However, there are still several challenges to be addressed. There is orders of magnitude energy efficiency difference between natural intelligence and artificial intelligence. Their suitability in mission critical applications is still in question -- they are vulnerable to adversarial attacks, while the results obtained from such systems are not yet fully explainable and verifiable. In this talk I will present some of

the latest developments (and challenges) in brain-guided algorithms and hardware that can make deep learning systems more efficient and robust.

SHORT BIO:

Dr. Kaushik Roy is the Edward G. Tiedemann, Jr., Distinguished Professor of Electrical and Computer Engineering at Purdue University. He received his PhD from University of Illinois at Urbana-Champaign in 1990 and joined the Semiconductor Process and Design Center of Texas Instruments, Dallas, where he worked for three years on FPGA architecture development and low-power circuit design. His current research focuses on cognitive algorithms, circuits and architecture for energy-efficient cognitive computing, computing models, and neuromorphic devices. Kaushik has supervised 75 PhD dissertations and his students are well placed in universities and industry. He is the co-author of two books on Low Power CMOS VLSI Design (John Wiley & McGraw Hill). He has received several best paper awards. Dr. Roy is a fellow of IEEE and he is on the editorial boards of several IEEE journals.

2

Software Defined Chips: An Innovative Architecture Leading to Intelligent Computing



Shaojun Wei
*Director, Institute
of Microelectronics,
Tsinghua University*

ABSTRACT:

Intellectualization is a revolution that human society is experiencing, and it is also the core of the fourth industrial revolution. Obviously it ultimately depends on integrated circuit technology, because not only now, but also in the future for quite a long time, we cannot find other technologies that can replace integrated circuits. Therefore, we have no other options than using integrated circuit technology for implementing intelligence. It is also the

reason why people spend a lot of energy focusing on AI chips in the development of artificial intelligence. For a large number of artificial neural networks each of which corresponds to only one application, an integrated circuit that cannot be changed after manufacturing is obviously far from the requirements. Even devices such as FPGA, which are field programmable, can hardly meet the needs of AI development in terms of computing efficiency and energy efficiency. We urgently need to find an innovative chip architecture. This paper will focus on software definition chip (SDC), an innovative chip architecture that allows the chip function to dynamically change in real time with the change of software. SDC moves from traditional software adapting hardware to hardware adapting software. By gradually improving the intelligence of chip, SDC eventually moves to intelligent chip. Besides, the core of SDC is a dynamically reconfigurable PE array that not only has high computing efficiency and energy efficiency, but also improves the reliability of the chip through redundant design, and improve the ability to resist attacks by randomly configuring the space-time position of the sensitive circuits as well. In addition, based on dynamic reconfigurability, the potential security threats caused by test paths in DFT are also mitigated.

SHORT BIO:

Dr. Shaojun Wei is the professor of Tsinghua University and currently serves as the Dean of the Department of Micro- and Nano-Electronics and Director of the Institute of Microelectronics, Tsinghua University.

He is also the adjunct professor of Peking University. Prof. WEI is the Vice President of the China Semiconductor Industry Association (CSIA), President of VLSI Design Chapter, CSIA. Prof. WEI is the President of Communication Specific IC Committee, China Institute of Communications (CIC) and the fellow of China Institute of Electronics (CIE). Prof. WEI is the chief scientist of State Key program of science and technology for integrated circuits.

3

Hold the reins in test engineering



Jochen Müller

Director for all ASIC test developments at Bosch GmbH

ABSTRACT:

The lecture describes recent and upcoming trends in the automotive industry with its derived automotive ASIC requirements and drivers behind. In addition some pitfalls in requirements engineering with respect to customer needs, specifications and test realisation are presented. A supporting toolset is discussed to achieve a continuous flow and control of requirements

starting with the customer specification, followed by datasheet and ending in testing software. As an example, an eclipse based toolchain is presented with dedicated features for requirements control including automatic code generation of test programs out of this tool. This code supports efficient installation and execution on selected modern test systems.

SHORT BIO:

Dr. Jochen Müller joined Robert Bosch GmbH in 1996 and started in the technology area. He was head of the production wafer test facility of Bosch until he became director for all ASIC test developments within Robert Bosch's semiconductor development in Reutlingen/Germany in 2012. His main focus is currently set to Bosch's international test technology network. Prior to joining Robert Bosch GmbH, Jochen Müller got his PhD at University of Dortmund. He studied electrical engineering with key aspects on microelectronics.

Talk to our experts
at ETS 2019 and
find out more



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Panels

TUESDAY, MAY 28, 2019

18:00 - 19:30 SESSION 5: Wine and Cheese Panel

Organizer and Moderator: Jeff REARICK, AMD - US

The Test Industry Roadmap: Ask the Experts!

We'll continue our tradition of tapping the collective expertise of the ETS participants by hosting an interactive "Ask The Experts" session during the Wine and Cheese Panel. The twist is that anyone can ask a question and _everyone_ has the chance to be the expert who answers it (or contests the answer of another expert). The general theme is "The Test Industry Roadmap" but anything goes. Prizes will be awarded for best question, best answer, and best rebuttal.

WEDNESDAY, MAY 29, 2019

13:30 - 15:00 SESSION 9A: Panel

Organizer: Harry Chen, MediaTek - TW

System-level Test (SLT) - What does the Future Hold?

Panelists: John YI, AMD - US

Marc HUTNER, Teradyne - CA

Anil BHALLA, Advantest - US

Carsten OHLHOFF, Continental Automotive - DE

Adit SINGH, Auburn University - US

Paolo BERNARDI, Politecnico di Torino - IT

Summary:

Testing of complex electronics-based systems is becoming more difficult and costly. To meet the challenge, can we count on enhanced structural test using advanced fault models such as

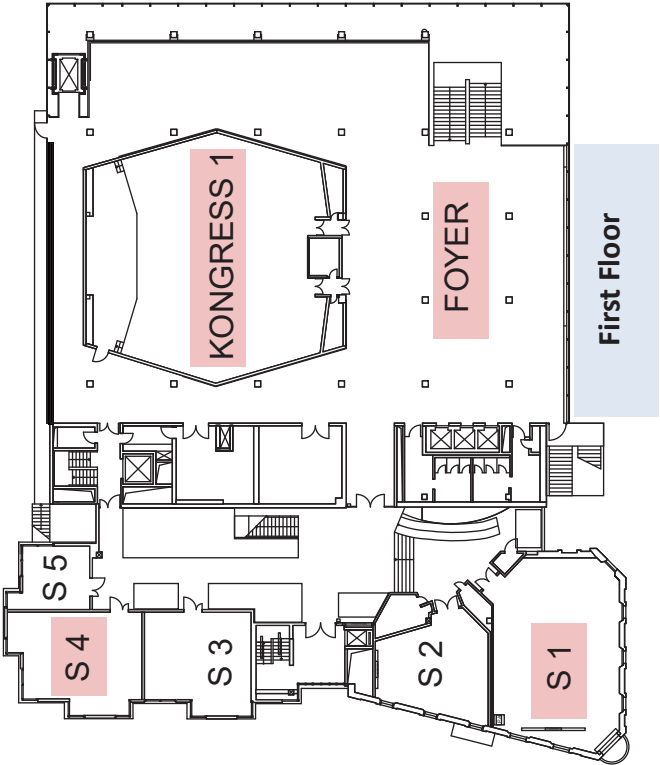
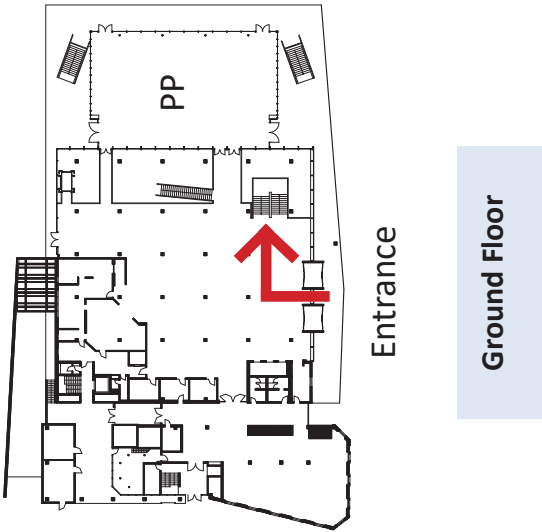
cell-aware? Or do we have to employ more system-level test (SLT)? Can a more methodical and standardized approach to SLT over current ad hoc practices be developed to achieve better cost efficiency? What about balancing the roles of traditional ATE and SLT testers for a more optimal test flow. Perhaps bring more SLT content upstream to wafer probe or include structural test content as part of in-system test? Is end-to-end test data analytics the solution to closing the diagnostic loop to identify the root causes of field failures? Should we be paying more attention to the role of embedded software when modern complex systems fail? What academic research topics will build the foundation for future system-oriented testing? These questions and possible approaches will be examined and debated by a panel of experts from industry and academia.



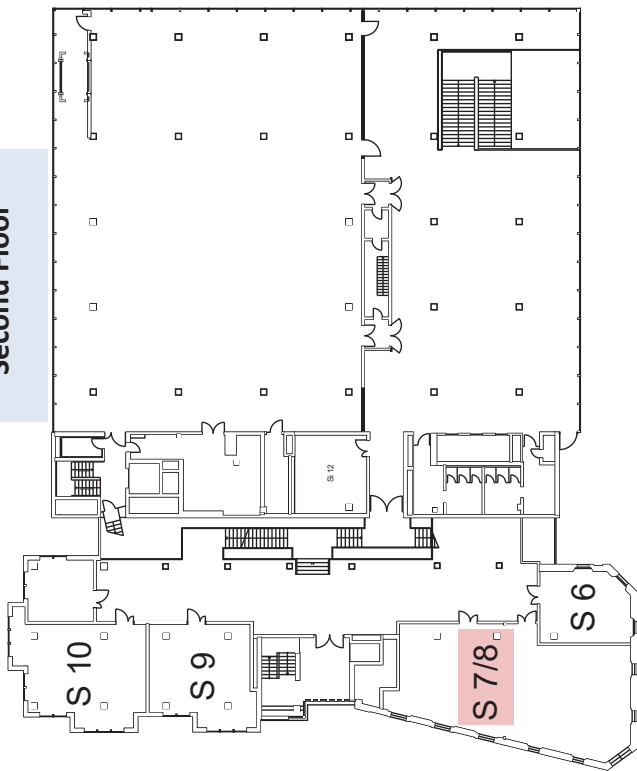
Baden, Baden Kur, & Tourismus GmbH

Casino

Map of the Venue



Second Floor



Legend:

KONGRESS 1 = Kongressaal 1
S1 = SITZUNG 1 = Sitzungsraum 1
S4 = SITZUNG 4 = Sitzungsraum 4
S7/8 = SITZUNG 7/8 = Sitzungsraum 7/8
PP = PARKPAVILLON

New Program Initiatives

This year ETS features two new program categories.

The Embedded Workshop targets work in progress as well as case studies. The sessions are characterized by an informal setup allowing for intensive interaction and lively discussions.

The PhD forum provides an excellent opportunity for PhD students to present their ongoing work and get feedback from experts in the field. It is organized as a special poster session on Tuesday afternoon. There will be an award for the best contribution to the Ph.D. Forum, which will be announced during the ETS'19 closing session.

Vendor Sessions

More information on the Vendor Sessions can be found online at

<https://www.testgroup.polito.it/ets19/vendor-session-presentations/>



Kongresshaus

Baden-Baden Kur & Tourismus GmbH

Program

MONDAY, MAY 27, 2019

14:00 - 16:00 TSS@ETS TUTORIAL A*: PART 1 SITZUNG 1

Analog, Mixed-Signal, RF IC Testing: Essentials and Current Trends
Harlampos STRATIGOPOULOS, *Sorbonne University - LIP6, FR*

14:00 - 16:00 TSS@ETS TUTORIAL B*: PART 1 SITZUNG 7/8

System-Level Test
Harry CHEN, *MediaTek - TW*

16:00 - 16:30 Coffee Break FOYER

16:30 - 18:30 TSS@ETS TUTORIAL A*: PART 2 SITZUNG 1

Analog, Mixed-Signal, RF IC Testing: Essentials and Current Trends
Harlampos STRATIGOPOULOS, *Sorbonne University - LIP6, FR*

16:30 - 18:30 TSS@ETS TUTORIAL B*: PART 2 SITZUNG 7/8

System-Level Test
Harry CHEN, *MediaTek - TW*

18:30 - 19:00 Break FOYER

19:00 - 21:00 Welcome Reception KURHAUS
See page 44 for more information

*The TSS@ETS Tutorials of Monday afternoon are accessible to all ETS attendees with a full registration.

TUESDAY, MAY 28, 2019

9:00 - 9:30 OPENING SESSION

KONGRESS 1

Opening Ceremony

Awards

9:30 - 10:15 SESSION 1 - KEYNOTE 1

KONGRESS 1

Moderator: Mehdi TAHOORI, *KIT - DE*

Cognitive Computing: Design, Verification & Security Challenges

Kaushik ROY, *Purdue University - US*

10:15 - 11:00 Coffee Break

FOYER

10:00 - 11:00 POSTER SESSION 1

FOYER

On the Evaluation of the PIPB Effect within SRAM-based FPGAs

Corrado DE SIO, Sarah AZIMI, Luca STERPONE, *Politecnico di Torino - IT*

B-open: A New Defect in Nanometric Technologies due to SADP Process

Freddy FORERO¹, Michel RENOVELL², Victor CHAMPAC¹

¹INAOE - MX, ²LIRMM - FR

Test Solutions for High Density 3D-IC Interconnects - Focus on SRAM-on-Logic Partitioning

Imed JANI, Pascal VIVET, Jean DURUPT, Sebastien THURIES,

Didier LATTARD, Edith BEIGNE, *CEA-LETI - FR*

Feature Engineering for Recycled FPGA Detection Based on WID Variation Modeling

Faisal AHMED, Michihiro SHINTANI, Michiko INOUE

Nara Institute of Science and Technology (NAIST) - JP

DFT Scheme for Hard-to-Detect Faults in FinFET SRAMs

Guilherme Cardoso MEDEIROS¹, Mottaqiallah TAOUIL¹,

Moritz FIEBACK¹, Leticia Bolzani POEHLIS², Said HAMDIOUI¹

¹Delft University of Technology - NL,

²Catholic University of Rio Grande do Sul - BR

11:00 - 12:30 SESSION 2A: Security

KONGRESS 1

Moderators: Subhasish MITRA, *Stanford University - US*
Johanna SEPULVEDA, *TUM - DE*

Inter-Lock: Logic Encryption for Processor Cores Beyond Module Boundaries

Dominik SISEJKOVIC¹, Farhad MERCHANT¹, Rainer LEUPERS¹,
Gerd ASCHEID¹, Sascha KEGREISS²

¹*RWTH Aachen - DE*, ²*Hensoldt Cyber GmbH - DE*

On Integrating Lightweight Encryption in Reconfigurable Scan Networks

Benjamin THIEMANN¹, Linus Feiten¹, Pascal RAIOLA¹,
Bernd BECKER¹, Matthias SAUER²

¹*University of Freiburg - DE*, ²*Advantest - DE*

Revisiting Logic Locking for Reversible Computing

Nimisha LIMAYE, Muhammad YASIN, Ozgur SINANOGLU
New York University Abu Dhabi - AE

11:00 - 12:30 SESSION 2B: Analog and Mixed Signal Test

SITZUNG 1

Moderators: Hans KERKHOFF, *University of Twente - NL*
Haralampos STRATIGOPOULOS,
Sorbonne University - LIP6 - FR

A 52 dB-SFDR 166 MHz Sinusoidal Signal Generator for Mixed-Signal BIST Applications in 28 nm FDSOI technology

Hani MALLOUG, Manuel BARRAGAN, Salvador MIR, *TIMA - FR*

Power Measurement and Spectral Test of ZigBee Transmitters from 1-bit Under-sampled Acquisition

Thibault VAYSSADE¹, Florence AZAÏS², Laurent LATORRE²,
Francois LEFEVRE¹, ¹*NXP - FR*, ²*LIRMM - FR*

Model-driven AMS Test Setup Validation Tool Prepared for IEEE P1687.2

Leon VAN DE LOGT¹, Vladimir ZIVKOVIC², Ingrid VAN BAAST¹
¹*D4T Systems - NL*, ²*Cadence - UK*

24th IEEE European Test Symposium 2019 – Program at a Glance

	Monday (May 27)	Tuesday (May 28)	Wednesday (May 29)	Thursday (May 30)	Friday (May 31)
08 : 30					Fringe Workshop
08 : 45					Fringe Workshop
09 : 00		Opening Session	Keynote 2: Shaojun Wei	Keynote 3: Jochen Müller	TESTA
09 : 15			Session 7A Memory	Session 11A AxC & Neuro-morphic	TruDevice
09 : 30			Session 7B Vendor	Session 11B Vendor	
09 : 45		Keynote 1: Kaushik Roy	Session 7C Embedded Workshop	Session 11C Embedded Tutorial	
10 : 00					
10 : 15					Fringe Workshop
10 : 30		Coffee Break + Poster 1	Coffee Break + Poster 2	Coffee Break + Poster 3	Joint Shiva/TruDevice
10 : 45					
11 : 00					
11 : 15		Session 2A Security	Session 8A Modelling, Validation and Verification	Session 12A DFT and BIST for 3D and AMS	
11 : 30		Session 2B Analog and Mixed Signal Test	Special Session 8B Security in Autonomous Systems	Session 12B Vendor	
11 : 45		Session 2C ETS ²	Session 8C Embedded Workshop	Session 12C Dependable Wireless IoT	
12 : 00					
12 : 15					
12 : 30					Fringe Workshop
12 : 45					Shiva
13 : 00			Lunch Break	Lunch Break	
13 : 15		Lunch Break			
13 : 30					
13 : 45					
14 : 00					

TUESDAY, MAY 28, 2019

11:00 - 12:30 SESSION 2C: ETS²

SITZUNG 7/8

Functional Safety and DFT –
Overlap or Conflict?

Moderators: Pete HARROD, *ARM - UK*

Zebo PENG, *Linköping University - SE*

Presenters: Teresa MCLAURIN, *ARM - US*

Jan SCHAT, *NXP Semiconductors - DE*

Michael SCHREINER, *Infineon - DE*

12:30 - 14:00 Lunch Break

PARKPAVILLON

14:00 - 15:30 SPECIAL SESSION 3A:

KONGRESS 1

Maintaining Automotive Quality for
Next Generation Microcontrollers

Organizer and Moderator: Daniel TILLE, *Infineon Technologies - DE*

Presenters:

Vladimir LITOVITCHENKO, *Synopsys - DE*

Ralf ARNOLD, *Infineon Technologies - DE*

Johanna SEPULVEDA, *TU-Munich - DE*

14:00 - 15:30 SESSION 3B: McCluskey

SITZUNG 1

Doctoral Thesis Award – ETS Semi-Finals

Moderators: Alberto BOSIO, *École Centrale de Lyon - FR*

Said HAMDIOUI, *TU Delft - NL*

15:30 - 16:15 Coffee Break

FOYER

A Methodology for Characterization and Mitigation of SET Effects in Combinational LogicMarko ANDJELKOVIC, Milos KRSTIC, Rolf KRÄMER, *IHP - DE***Programmable In-Situ Delay Monitor for Energy-Efficient and Resilient Complex SoC**Mitko VELESKI, Rolf KRÄMER, Milos KRSTIC, *IHP - DE***Dependability of Safety-Critical Automotive SoC**Marco RESTIFO, *Politecnico di Torino - IT***A boot-time self-test procedures scheduler for multi-core automotive System-on-Chips**Andrea FLORIDIA, *Politecnico di Torino - IT***Self-Adaptive Cross-Layer Fault Tolerance in Multiprocessor Systems**Junchao CHEN, Milos KRSTIC, *IHP - DE***SAT modulo differential equations**Tomas KOLARIK, Stefan RATSCHAN, *CTU Prague - CZ***Encryption Techniques for Test Infrastructures**Emanuele VALEA¹, Marie-Lise FLOTTES¹, Giorgio DI NATALE², Bruno ROUZEYRE¹, ¹LIRMM - FR, ²TIMA - FR**On the Evaluation of SET-induced Errors on Dynamically Reconfigurable FPGAs**Corrado DE SIO, Ludovica BOZZOLI, Sarah AZIMI, Luca STERPONE
*Politecnico di Torino - IT***Verifying IEEE 1687 ICL against RTL –****Code Coverage and Functional Coverage**Aleksa DAMLIJANOVIC, *Politecnico di Torino - IT***Efficient hardening solutions on GPUs for safety critical applications**Fernando Fernandes DOS SANTOS, Paolo RECH
*Universidade Federal do Rio Grande do Sul - BR***Embedded System back-annotation by qualifying component model template**Katayoon BASHARKHAH, *University of Tehran - IR***Machine Learning to Tackle the Challenges of Transient and Soft Errors in Complex Circuits**Thomas LANGE¹, Aneesh BALAKRISHNAN¹, Maximilien GLORIEUX¹, Dan ALEXANDRESCU¹, Luca STERPONE²¹iRoC Technologies, ²Politecnico di Torino - IT**Learning Enhanced Diagnosis of Logic Circuit Failures**Soumya MITTAL, Shawn BLANTON, *Carnegie Mellon University - US***Vector-IR-based translation approach of pattern programs**Jung-Geun PARK, Minsu KIM, *Seoul National University - KR*

16:15 - 17:45 SESSION 4A: Test Generation KONGRESS 1

Moderators: Grzegorz MRUGALSKI, *Mentor, a Siemens Business - PL*
Melanie SCHILLINSKY, *NXP - DE*

Machine Learning-based Prediction of Test Power

Harshad DHOTRE¹, Stephan EGGERSGLUESS²,
Krishnendu CHAKRABARTY³, Rolf DRECHSLER¹
¹*University of Bremen - DE*, ²*Mentor, a Siemens Business - DE*,
³*Duke University - US*

On Generating Fault Diagnosis Patterns for Designs with X Sources

Xijiang LIN¹, Sudhakar REDDY²
¹*Mentor, a Siemens Business - US*, ²*University of Iowa - US*

High-Level Combined Deterministic and Pseudoexhaustive Test Generation for RISC Processors

Adeboye OYENIRAN, Raimund UBAR, Maksim JENIHHIN, Cemil Cem GURSOY, Jaan RAIK, *Tallinn University of Technology - EE*

16:15 - 17:45 SESSION 4B: Fault Tolerance SITZUNG 1

Moderators: Valentin GHERMAN, *CEA - FR*
Huang ZHENGFEI, *Hefei University of Technology - CN*

IJTAG Compatible Timing Monitor with Robust Self-Calibration for Environmental and Aging Variations

Ghazanfar ALI, Jerrin PATHROSE, Hans KERKHOFF
University of Twente - NL

STAHL: A Novel Scan-Test-Aware Hardened Latch Design

Ruijun MA¹, Stefan HOLST¹, Xiaoqing WEN¹, Aibin YAN², Hui XU²
¹*Kyushu Institute of Technology - JP*, ²*Anhui University - CN*

Hardware-Based Aging Mitigation Scheme for Memory Address Decoder

Daniel KRAAK¹, Innocent AGBO¹, Mottaqiallah TAOUIL¹, Said HAM-DIOUI¹, Pieter WECKX², Stefan COSEMANS², Francky CATTLOOR²
¹*Delft University of Technology - NL*, ²*IMEC - BE*

17:45 - 18:00 Break FOYER

18:00 - 19:30 SESSION 5: Wine and Cheese Panel KONGRESS 1

Organizer and Moderator: Jeff REARICK, *AMD - US*

The Test Industry Roadmap: Ask the Experts!

For more information see page 16.

19:30 - 21:30 Networking Grill PARKPAVILLON

For more information see page 42.

WEDNESDAY, MAY 29, 2019

8:30 - 9:15 SESSION 6: Keynote 2 KONGRESS 1

Moderator: Krishnendu CHAKRABARTY, *Duke University - US*
Software Defined Chips: An Innovative Architecture Leading to Intelligent Computing
Shaojun WEI, *Tsinghua University - CN*

9:15 - 10:15 SESSION 7A: Memory KONGRESS 1

Moderators: Michele STUCCHI, *IME - BE*
Ioana VATAJELU, *TIMA - FR*

Pinhole Defect Characterization and Modeling for STT-MRAM Testing
Lizhou WU¹², Siddharth RAO², Guilherme Cardoso MEDEIROS¹, Mottaqiallah TAOUIL¹, Erik Jan MARINISSEN², Farrukh YASIN², Sebastien COUET², Said HAMDIOUI¹, Gouri Sankar KAR²
¹*Delft University of Technology - NL*, ²*IMEC - BE*
A Machine Learning based Approach to Optimize Repair of Embedded Flash Memories in Automotive System-on-Chip
Andrea MANZINI¹³, Pietro INGLESE²⁴, Leonardo CALDI⁴, Riccardo CANTORO², Giambattista CARNEVALE³, Matteo COPPETTA³, Massimo GILTRELLI³, Nellina MAUTONE³, Fernanda IRRERA¹, Rudolf ULLMANN⁴, Paolo BERNARDI²
¹*University of Rome - IT*, ²*Politecnico di Torino - IT*, ³*Infineon - IT*, ⁴*Infineon - DE*

9:15 - 10:15 SESSION 7B: Vendor Session SITZUNG 7/8

Moderator: Hans MANHAEVE, *Ridgetop Europe - BE*
Test and Repair for SoC Memories and Hierarchical Test for AMS & PHY IP
Yervant ZORIAN, *Synopsys Fellow - US*
Advantest and EDA: Partnering to Deliver Customer Values
Michael BRAUN, *Advantest - DE*

9:15 - 10:15 SESSION 7C: Embedded Workshop: Case Studies SITZUNG 1

Moderator: Gildas LEGER, *IMSE-CNM - ES*
Flight Safety Certification Implications for Complex Multi-Core Processor based Avionics Systems
Jyotika ATHAVALA¹, Riccardo MARIANI², Michael PAULITSCH³
¹*Intel Corporation - US*, ²*Intel Corporation - IT*, ³*Intel Corporation - DE*
Hybrid Verification Methodology for Automotive RADAR
Shiva NEGENDAR, Sainath KARLAPALEM, Paulraj KANAKARAJ, Shank VENUGOPAL, *NXP - IN*

WEDNESDAY, MAY 30, 2018

10:15 - 11:00 Coffee Break

FOYER

10:15 - 11:00 POSTER SESSION 2

FOYER

Concurrent Estimation of a PLL Transfer Function by Cross-Correlation with pseudo-random Jitter

Jan SCHAT, Ulrich MÖHLMANN, *NXP Semiconductors - DE*

PaTran: a Translation Platform for Test Pattern Programs

Jung-Geun PARK¹, Minsu KIM¹, Sungyeol KIM², Insu YANG²,
Hyunsoo JUNG², Soo-Mook MOON²

¹Seoul National University - KR, ²Samsung Electronics Co., Ltd. - KR

A Functional Approach to Test and Debug of IEEE 1687

Reconfigurable Networks

Michele PORTOLAN¹, Riccardo CANTORO², Ernesto SANCHEZ²

¹TIMA - FR, ²Politecnico di Torino - IT

Test Adapted Shielding by a Multipurpose Crosstalk Avoidance Scheme

Mahsa AKHSHAM, Atefesadat SEYEDOLHOSSEINI,

Zainalabedin NAVABI, *University of Tehran - IR*

Hybrid Architecture for Embedded Test Compression to Process Rejected Test Patterns

Sebastian HUHN¹, Daniel TILLE², Rolf DRECHSLER³

¹DFKI GmbH - DE, ²Infineon - DE, ³University of Bremen/DFKI - DE

11:00 - 12:30 SESSION 8A: Modeling, Validation
and Verification

KONGRESS 1

Moderators: Bernd BECKER, *University of Freiburg - DE*

René KRENZ-BAATH, *Hamm-Lippstadt University of Applied Sciences - DE*

Back-Annotation of Interconnect Physical Properties for System-Level Crosstalk Modeling

Zainalabedin NAVABI, Rezgar SADEGHI, Nooshin NOSRATI,
Katayoon BASHARKHAH, *University of Tehran - IR*

Post-Silicon Validation of IEEE 1687 Reconfigurable Scan Networks

Aleksa DAMLIJANOVIC¹, Artur JUTMAN², Giovanni SQUILLERO¹,
Anton TSERTOV², ¹Politecnico di Torino - IT, ²Testonica Lab - EE

Exploring Algebraic Interpolants for Rectification of Finite Field Arithmetic Circuits with Groebner Bases

Utkarsh GUPTA¹, Priyank KALLA², Irina ILIOAEA², Florian ENESCU²
¹University of Utah - US, ²Georgia State University - US



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Theater

WEDNESDAY, MAY 30, 2018

11:00 - 12:30 SPECIAL SESSION 8B:

SITZUNG 7/8

Security in Autonomous Systems

Organizer and Moderator: Ilia POLIAN, *University of Stuttgart - DE*

Presenters:

Francesco REGAZZONI, *University of Lugano - CH*

Marc STÖTTINGER, *Continental AG - DE*

Stefan KATZENBEISSER, *TU-Darmstadt - DE*

11:00 - 12:30 SESSION 8C: Embedded Workshop:

SITZUNG 1

Advances in DfT

Moderators: Jochen Rivoir, *Advantest - DE*

Matthias Sauer, *Advantest - DE*

Architecture for fast and precise and Voltage Measurement for Analog Test Points

Jan Schat, *NXP Semiconductors - DE*

Facilitating Memory Test Using Shared Bus Interface

Albert AU¹, Sebastian BROMBEREK², Martin KEIM³,

Benoit NADEAU-DOSTIE¹, Artur POGIEL²

¹Mentor, a Siemens Business - CA, ²Mentor, a Siemens Business - PL,

³Mentor, a Siemens Business - US

Novel Clock and Reset DFT Methods to Improve Hierarchical ATPG Pattern Reuse Shown on a GPU Design

Beomseok SHIN², Jinsoo PARK², Jungyul PYO², Youngmin SHIN²,

Ron PRESS¹, Takeo KOBAYASHI¹, Yoon Dong LEE³, Inchul KIM³

¹Mentor, a Siemens Business - US, ²Samsung Electronics - KR,

³Mentor, a Siemens Business - KR

12:30 - 14:00 Lunch Break

PARKPAVILLON



*Geroldsauer
Mühle*

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14:00 - 15:30 SESSION 9A: Panel
System-level Test (SLT) -
What does the Future Hold?

SITZUNG 7/8

Organizer: Harry Chen, MediaTek - TW

Panelists: John YI, *AMD - US*
Marc HUTNER, *Teradyne - CA*
Anil BHALLA, *Advantest - US*
Carsten OHLHOFF, *Continental Automotive - DE*
Adit SINGH, *Auburn University - US*
Paolo BERNARDI, *Politecnico di Torino - IT*

For more information see page 16

14:00 - 15:00 SESSION 9B: Embedded Tutorial:
Alternatives to Fault Injections for
Early Safety/Security Evaluations

SITZUNG 1

Organizer and Moderator: Régis LEVEUGLE, *TIMA - FR*

Presenters:
Régis LEVEUGLE, *TIMA - FR*
Michele PORTOLAN, *TIMA - FR*
Stefano DI CARLO, *Politecnico di Torino - IT*

15:30 - 16:30 Break

16:30 - 22:00 Social Event
See page 42 for more information.

ENTRANCE

THURSDAY, MAY 30, 2019

8:30 - 9:15 SESSION 10: Keynote 3

KONGRESS 1

Moderator: Hans-Joachim WUNDERLICH, *University of Stuttgart - DE*

Hold the reins in test engineering

Jochen Müller, *Bosch - DE*

9:15 - 10:15 SESSION 11A: Approximate and

KONGRESS 1

Neuromorphic Computing

Moderators: Rohit KAPUR, *Cadence - US*

Adit SINGH, *Auburn University - US*

Approximate computing design exploration through data lifetime metrics

Alessandro SAVINO¹, Michele PORTOLAN², Régis LEVEUGLE², Stefano DI CARLO¹, ¹*Politecnico di Torino - IT*, ²*TIMA - FR*

Impact of Reduced Precision in the Reliability of Deep Neural Networks for Object Detection

Fernando Fernandes DOS SANTOS, Philippe NAVAUX, Luigi CARRO, Paolo RECH, *Universidade Federal do Rio Grande do Sul - BR*

8:30 - 9:15 SESSION 11B: Vendor Session

SITZUNG 7/8

Moderator: Pete HARROD, *ARM - UK*

Mini-Tutorial: The (black) art of current test

Hans Manhaeve, *CEO Ridgetop Europe - BE*

8:30 - 9:15 SESSION 11c: Embedded Tutorial:

SITZUNG 1

Connecting the Dots: How IEEE P1687.1, P1687.2, and IEEE P2427 Play Together

Organizer: Martin KEIM, *Mentor, a Siemens Business - US*

Moderator: Jeff REARICK, *AMD - US*

Presenters:

Martin KEIM, *Mentor, a Siemens Business - US*

Jeff REARICK, *AMD - US*

Vladimir ZIVKOVIC, *Cadence - UK*

10:15 - 11:00 Coffee Break

FOYER

10:15 - 11:00 POSTER SESSION 3

FOYER

**Test Pattern Generator for Majority Voter based QCA
Combinational Circuits targeting MMC Defect**

Vaishali DHARE, Usha MEHTA, *Nirma University - IN*

Symbolic Circuit Analysis under an Arc Based Timing Model

Goerschwin FEY¹, Alberto GARCIA-ORTIZ²

¹TU Hamburg - DE, ²University of Bremen - DE

**A Dynamic Greedy Test Scheduler for Optimizing
Probe Motion in In-Circuit Testers**

Matteo Sonza Reorda¹, Giovanni Squillero¹, Luciano Bonaria²,
Maurizio Raganato², ¹Politecnico di Torino - IT, ²SPEA - IT

11:00 - 12:30 SESSION 12A: DfT and BIST
for 3D and AMS

KONGRESS 1

Moderators: Jürgen ALT, *Intel - DE*

Erik Jan MARINISSEN, *IMEC - BE*

**Digital Built-in Self-Test for Phased Locked Loops to
Enable Fault Detection**

Mehmet INCE, Sule OZEV, *Arizona State University - US*

Built-in Self-Test for Inter-Layer Vias in Monolithic 3D ICs

Arjun CHAUDHURI¹, Sanmitra BANERJEE¹, Heechun PARK²,
Bon Woong KU², Krishnendu CHAKRABARTY¹, Sung Kyu LIM²

¹Duke University - US, ²Georgia Institute of Technology - US

**K^Λ3 TAM Optimization for Testing 3D-SoCs using Non-Regular
Time-Division-Multiplexing**

Panagiotis GEORGIU, Iakovos THEODOSOPOULOS,
Chrysovalantis KAVOUSIANOS, *University of Ioannina - GR*

11:00-12:30 Session 12B – Vendor Session

SITZUNG 7/8

Moderator: Jürgen SCHLÖFFEL, *Mentor, a Siemens Business - DE*

Moving DFT solutions to the next level

Kan THAPAR, *Mentor, a Siemens Business - UK*

IP Solutions for Functional Safety Applications

Pete HARROD, *Director of Functional Safety, CPU Group, ARM - UK*

**ProChek Plus – A solution for Process assessment from a quality/
reliability perspective**

Hans MANHAEVE, *CEO Ridgetop Europe - BE*

THURSDAY, MAY 30, 2019

11:00 - 12:30 SPECIAL SESSION 12C:

Dependable Wireless Industrial IoT

SITZUNG 1

Organizers: Fotis FOUKALAS and Paul POP, *TU-Denmark - DK*

Moderator: Fotis FOUKALAS, *TU-Denmark - DK*

Presenters:

Fabrice THEOLEYRE, *CNRS - FR*

Carlo Alberto BOANO, *TU-Graz - AT*

Chiara BURATTI, *University of Bologna - IT*

Fotis FOUKALAS, *TU-Denmark - DK*

12:30 - 14:00 Lunch Break

PARKPAVILLON

14:00 - 15:30 SESSION 13: Diagnosis

KONGRESS 1

Moderators: Sybille HELLEBRAND, *University of Paderborn - DE*

Stefan HOLST, *Kyushu Institute of Technology - JP*

A Supervised Machine Learning Application in Volume Diagnosis

Yue TIAN¹, Gaurav VEDA², Wu-Tung CHENG², Manish SHARMA²,

Huaxing TANG², Neerja BAWASKAR³, Sudhakar REDDY¹

¹*University of Iowa - US*, ²*Mentor, a Siemens Business - US*,

³*Globalfoundries - US*

Non-Adaptive Pattern Reordering to Improve

Scan Chain Diagnostic Resolution

Yu HUANG, Jakub JANICKI, Szczepan URBAN

Mentor, a Siemens Business - US

LearnX: A Hybrid Deterministic-Statistical

Defect Diagnosis Methodology

Soumya Mittal, Shawn Blanton, *Carnegie Mellon University - US*

15:30 - 16:00 CLOSING SESSION

KONGRESS 1

18:00 - 19:00 Workshop Reception

FOYER

See page 38 for more information.



Stadtmuseum

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Festspielhaus



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FRINGE Workshops

The following workshops are co-located with ETS'19 and will run in parallel, starting Thursday May 30 at 16:00, ending Friday May 31 at 15:30/18:00. There will be a workshop reception for the workshop attendees on Thursday May 30 at 18:00, which takes place in 1st floor Foyer between SITZUNG 1 and SITZUNG 4.

TESTA'19

4th International Test Standards Application Workshop

General Chair: Michele PORTOLAN, *TIMA - Grenoble, FR*

Room: SITZUNG 4

The TESTA workshop is a focused, open discussion platform dedicated to exchange of fresh ideas, industrial best practices, methodologies and work-in-progress around test related standards, especially those being actively developed today or the ones recently released. Contributions covering IEEE 1149.x, IEEE 1500, IEEE 1687, IEEE 1450, and open Working Groups like IEEE P1838, IEEE P1687.x and STAM are expected. Particularly welcome are contributions that discuss what works, what does not, or how the standards were incorporated into existing or new DFT methodologies. Reports on first-time usage of new and upcoming standards are welcome, as is research exploring the best usage of features described in these standards.

Further Information:

<https://www.testgroup.polito.it/ets19/testa2019/>

SHIVA:

Secure Hardware, Integrity and preVention of Attacks
Workshop

Organizers:

Hans-Joachim WUNDERLICH, *University of Stuttgart - DE*

Bernd BECKER, *University of Freiburg - DE*

Room: SITZUNG 1

The SHIVA Workshop will provide an environment for researchers and practitioners from academia and industry as well to discuss challenges, recent developments, and on-going work in hardware security, in particular w.r.t. topics like securing scan infrastructure against attacks, techniques to protect a system against (un)intentional manipulation and against reading out of confidential information or intellectual property.

Further Information:

[http://www.iti.uni-stuttgart.de/
lehre/ets-workshop-2019.html](http://www.iti.uni-stuttgart.de/lehre/ets-workshop-2019.html)

TRUDEVICE 2019

8th Workshop on Trustworthy Manufacturing and
Utilization of Secure Devices

General Chairs:

Francesco REGAZZONI, *ALaRI - USI - CH*

Giorgio DI NATALE, *CNRS - TIMA - Grenoble, FR*

Program Chairs:

Osnat KEREN, *Bar Ilan University - IL*

Stjepan PICEK, *Delft University of Technology - NL*

Room: SITZUNG 1

Hardware security is becoming increasingly important for many embedded systems applications ranging from small RFID tag to satellites orbiting the earth: secure applications such as public services, communication, control and healthcare keep growing, however hardware devices that implement cryptography functions has become the Achille's heel in the last decade. The TRUDEVICE Workshop will provide an environment for researchers from academic and industrial domains who want to discuss recent findings, theories and on-going work on all aspects of hardware security including design, manufacturing, testing, reliability, validation and utilization. Program will include invited talks, contributed talks and work in progress.

Further Information:

[https://www.testgroup.polito.it/ets19/
trudevice-workshop-call-for-contributions](https://www.testgroup.polito.it/ets19/trudevice-workshop-call-for-contributions)

FRINGE Meetings

ETS Steering Committee Meeting

Chair: Matteo SONZA REORDA

Room: SITZUNG 4

Monday, May 27, 16:00–19:00

ETS Steering Committee Meeting

Chair: Matteo SONZA REORDA

Room: SITZUNG 4

Tuesday, May 28, 12:30–14:00

ETTTTC Meeting

Chair: Alberto BOSIO

Room: SITZUNG 4

Wednesday, May 29, 12:30–13:30

About eTTTC:

The European Test Technology Technical Council (eTTTC) is the European section of the TTTC. eTTTC is a volunteer professional organization sponsored by the IEEE Computer Society.

TTTC's goals are to contribute to our members' professional development and advancement, to help them solve engineering problems in electronic test, and to help advance the state-of-the art.

This meeting provides all actors involved in test technology to share information on upcoming events and projects.

ETS2020 Executive Committee Meeting

Chairs: Artur JUTMAN and Jaan RAIK

Room: SITZUNG 4

Thursday, May 30, 12:30–14:00

Welcome Reception



The welcome reception of ETS 2019 takes place at Kurhaus Baden-Baden, next to the casino and overlooking the historical Trinkhalle. It is close to the conference venue, reachable in only five minutes by foot.

See the map on page 46/47 for the location.

The event will take place on Monday, May 27th, 2019 starting at 19:00.

Kurhaus Baden-Baden
Kaiserallee 1
D-76530 Baden-Baden

Networking Grill

After the panel discussion on Tuesday afternoon, all conference attendees are invited for a networking grill on the terrace of Parkpavillon (conference venue) for a get-together and networking with good food and drinks.

The event will take place on Tuesday, May 28th, 2019 starting at 19:30.



TEST FOR THE AUTONOMOUS AGE



Mentor's Tessent product line is the technology and market leading design-for-test solution. Tessent's RTL-based hierarchical DFT solution enables customers to achieve lower test cost, higher test quality, faster yield ramps and meet the functional safety requirements demanded by the automotive market's ISO 26262 standard.

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Social Activities

The main social event will be on Wednesday, May 29.

This year's social event starts at 16:30 in front of the conference venue with a guided tour through Baden-Baden. Afterwards we will go to Geroldsauer Mühle by bus and spend the rest of the evening there.

The departure of the buses will be at 18:30 in front of the venue entrance.

16:30 - 18:30 Guided walking tour of Baden-Baden

Discover Baden-Baden on this guided walking tour with the certified city guides and stroll through the elegant "Kurviertel" with its magnificent buildings like the "Kurhaus/Casino", the Theater and the "Trinkhalle" (Pump Room). Furthermore, you will get to know the traditional "Spa Quarter" and the historic "Old Town" of Baden-Baden as well as interesting facts and anecdotes.

Meeting point: 4.30 p.m., in front of the entrance of the Kongresshaus Baden-Baden (Augustaplatz 10).

English-speaking Baden-Baden guides will be waiting for you.

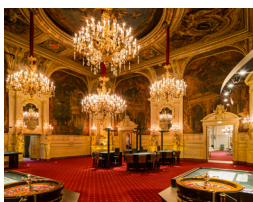
Duration of the walking tour: 1.5 – 2 hours



Trinkhalle



Brahms-Haus



Casino



Baden-Baden Kur & Tourismus GmbH

18:30 - 22:00 Geroldsauer Mühle

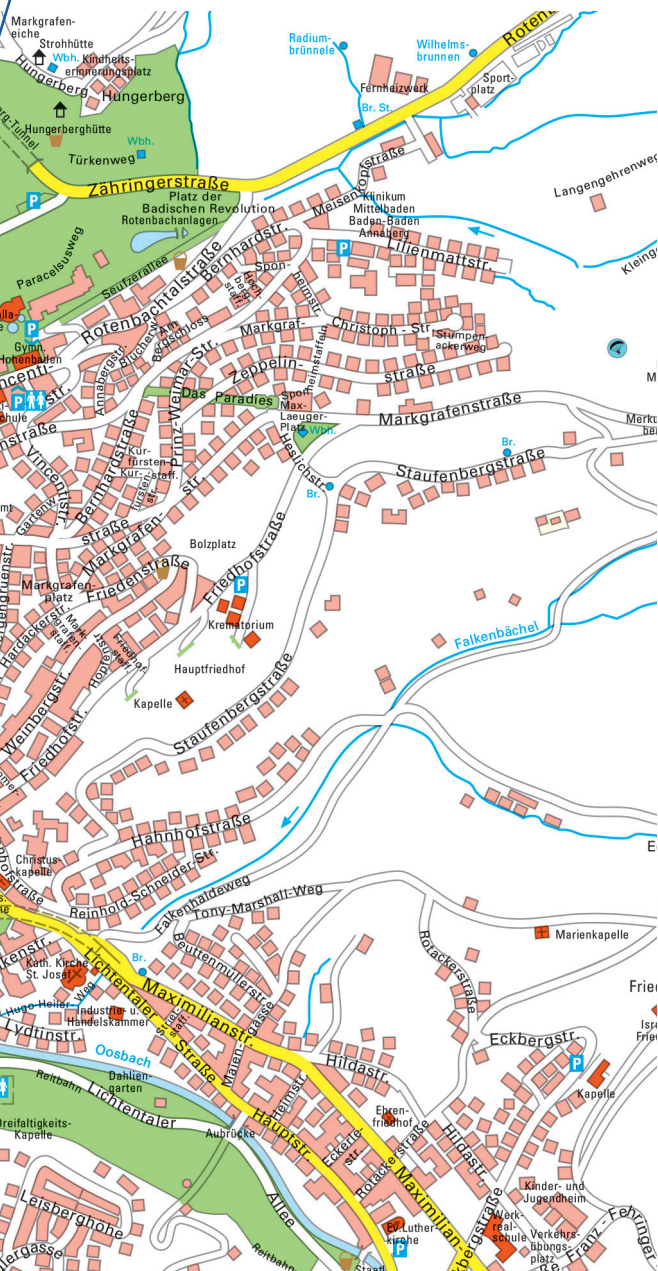
As gate to the Black Forest, the Geroldsauer Mühle (mill) is known thanks to its geographical location, as well as thanks to its offer to experience the Black Forest in its purest form.

This landmark is one of the largest silver fir buildings in the whole region. In the left wing, it disposes of a restaurant and an extensive beer garden in a scenic setting. Here you will find regional specialties and the hospitality so typical of Baden. The right wing of the building offers a mill market featuring a selection of regional and organic foods. You can watch the bakery right next door making baked goods using its own mill, the butcher of the mill market offering high-quality meats from select nature park businesses in the Black Forest or buy unique decorative goods and artistic works for your home. Finally, the Central/Northern Black Forest Nature Park, one of Germany's largest nature parks, as well as the Black Forest National Park and the municipality of Baden-Baden are represented on the second floor of the Geroldsauer Mühle with a varied exhibition on the region's attractions. Discover the Black Forest and its diverse natural and cultural landscape first-hand, looking at interesting images of woodlands, fields and meadows – and a range of further experiences.

Local Map

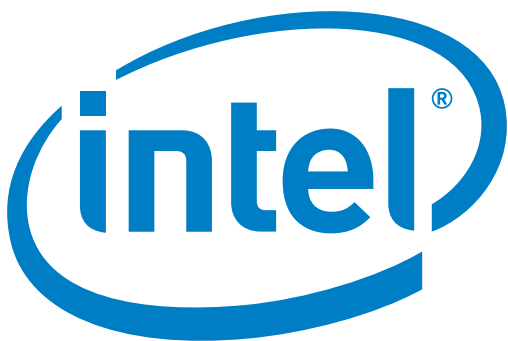
Welcome Reception / Kurhaus





NOTES

..... see you next year



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